DESIGN OF MULTIPLEXER USING ADIABATIC LOGIC

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ABSTRACT

This paper provides low power solutions for Very Large Scale Integration design. The dynamic power consumption of CMOS circuits is rapidly becoming a major concern in VLSI design. By adiabatic technique dynamic power consumption in pull up network can be reduced and energy stored on the load capacitance can be recycled. In this paper different logic style multiplexes have been analyzed and low power 2:1 multiplexer is designed using positive feedback adiabatic logic. It has been observed that adiabatic multiplexer consumes 53.1% less power than energy economized pass-transistor (EEPL) multiplexer. An adiabatic compressor has been designed using PFAL logic, which has shown 79% improvement than conventional CMOS compressor in terms of power.

KEYWORDS: *MUX, PFAL, CMOS, VLSI, BSIM4.*

I. INTRODUCTION

In today's world of portable devices such as laptops, cell phones, computer power consumption has become major concern in VLSI design. Due to the limited power supplied by the batteries, the circuitry involved in these devices must be designed to consume less power. Also large power dissipation requires expensive and noise cooling machinery, batteries and power conservation circuits.Multiplexer is essential component in digital design. It is extensively used within datapath-intensive designs. Thus minimizing the power dissipation of the multiplexer is one of the main concerns of low power design [1].

Most of the power saving techniques involved scaling of the power supply, which results, substantial increase in subthreshold leakage current also it causes uncertainty in the process variation. Therefore some other technique is required which is independent of voltage scaling. It has been found that there is fundamental connection between computation and power dissipation. That is if somehow computation could be implemented without any loss of information, then energy required by it could be potentially reduced to zero. This can be achieved by performing all the computation in a reversible manner. Thus minimum power consumption during charge transfer phase is known as adiabatic switching. Conventional CMOS based designs consume a lot of energy during switching process. Adiabatic switching technique reduces the energy dissipation through PMOS during charging process and reuses some of the energy which is stored on load capacitor during the discharging phase [2-3].